IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) A dynamic circuit comprising:

a clock input terminal;

a plurality of input terminals other than the clock input terminal;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively,

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and a second potential power supply, and

the precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node.

2. (Currently amended) A dynamic circuit comprising:

a first clock input terminal;

a second clock input terminal;

a plurality of input terminals other than the first clock input terminal and the second clock input terminal;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal;

a discharge MOS transistor connecting a source-drain path between a discharge node and a second potential power supply and connecting a gate terminal to the second clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively,

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and the discharge node, and

the precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node.

3. (Original) The dynamic circuit according to claim 1 or 2, wherein a clock signal applied to the clock input terminal connected to the gate terminal of the precharge MOS transistor is delayed so that the precharge MOS transistor is conducted even after the formation of the conductive path from the intermediate node to the precharge node.

4. (Currently amended) The dynamic circuit according to claim 1 or 2, wherein a clock signal applied to the clock input terminal connected to the gate terminal of the precharge MOS transistor is produced by performing a logical operation with an original clock signal ~~signals applied to the input terminals~~ so that the precharge MOS transistor is conductive ~~conducted~~ even after the formation of the conductive path from the intermediate node to the precharge node.

5-18. (Canceled)

19. (New) The dynamic circuit according to Claim 2,

wherein the precharge MOS transistor becomes conductive substantially at the same time when the discharge MOS transistor becomes non-conductive.

20. (New) The dynamic circuit according to Claim 19,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the precharge MOS transistor is produced by performing a logical operation of an original clock signal applied to the clock input terminal and its delayed signal.

21. (New) A dynamic circuit comprising:

a clock input terminal;

a plurality of input terminals other than the clock input terminal;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively,

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and a second potential power supply,

the precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node, and

the precharge MOS transistor becomes non-conductive after formation of a conductive path from the intermediate node to the second potential power supply.

22. (New) A dynamic circuit comprising:

a first clock input terminal;

a second clock input terminal;

a plurality of input terminals other than the first clock input terminal and the second clock input terminal;

a precharge MOS transistor connecting a source-drain path between a first potential power supply and a precharge node and connecting a gate terminal to the first clock input terminal;

a discharge MOS transistor connecting a source-drain path between a discharge node and a second potential power supply and connecting a gate terminal to the second clock input terminal; and

a plurality of logical-operating MOS transistors,

wherein gate terminals of the plurality of logical-operating MOS transistors are connected to one of the plurality of input terminals, respectively,

at least one intermediate node is formed to connect the source-drain paths of the plurality of logical-operating MOS transistors between the precharge node and the discharge node,

the precharge MOS transistor is conductive even after formation of a conductive path from the intermediate node to the precharge node, and

the precharge MOS transistor becomes non-conductive after formation of a conductive path from the intermediate node to the second potential power supply.

23. (New) The dynamic according to Claim 21 or 22,

wherein a clock signal applied to the clock input terminal connected to the gate terminal of the precharge MOS transistor is produced by performing a logical operation with an original clock signal and at least one signal applied to the plurality of input terminals.